Special Notice

Microsystems Exploration Research Area Announcement

DARPA-SN-19-69

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Defense Advanced Research Projects Agency
Microsystems Technology Office
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SPECIAL NOTICE DARPA-SN-19-69
Microsystems Exploration Research Area Announcement
TECHNICAL POC: Multiple PMs
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Background

The purpose of this Special Notice (SN) is to provide public notification of research areas of initial interest to the Microsystems Technology Office, specifically the Microsystems Exploration program. The Defense Advanced Research Projects Agency (DARPA) Microsystems Technology Office (MTO) seeks to develop high-risk, high-reward technologies that enable revolutionary advances in materials, devices, and systems and continue DARPA's mission of creating and preventing strategic surprise. In order to capitalize rapidly on new opportunities, DARPA announced the Microsystems Exploration program in July 2019 that calls for faster responses with smaller, targeted investments. Microsystems Exploration awards will be made within 90 days of each Microsystems Exploration topic announcement.

To enable this new approach, MTO will issue Microsystems Exploration Topics (called μE topics) via targeted Pre-Solicitation Notices. These Pre-Solicitation Notices will focus on technical domains important to MTO's mission pursuing innovative research concepts that explore frontiers in:

- Embedded microsystem intelligence and localized processing,
- Next-generation electromagnetic components and technologies,
- Microsystem integration for functional density and security, and
- Disruptive microsystem applications in command, control, communications computer, intelligence surveillance, and reconnaissance (C4ISR), electronic warfare, and directed energy.

Microsystems Exploration Topics (μEs)

As stated in the associated program announcement (PA) (see DARPA-PA-19-04), these μE topics will solicit proposals and will be open for at least 30 days from publication at https://www.fbo.gov (fbo.gov) Each μE topic published on fbo.gov will be numbered in the following format: DARPA-PA-19-04-XX (for example, the first μE topic will be numbered DARPA-PA-19-04-01). Each μE topic will (1) identify specific details regarding the research topic of interest, and (2) provide proposal and submission instructions in addition to those outlined in the PA, including the proposal due date. Interested parties should note that proposals must only be submitted in response to a μE topic. Proposals submitted in response to this Special Notice or to the Microsystems Exploration program announcement (DARPA-PA-19-04) will be disregarded.

The initial μE topics that are anticipated to be released between July 2019 and October 2019 are summarized below:

- **Board-Level Hardware Security:**
  The offshoring of the fabrication of information technology (IT) systems has recently been reported as a threat for the insertion of supply chain implants in commercial-off-the-shelf (COTS) hardware, such as internet routers and computer servers. The supply chain is complex and an individual component changes hands multiple times, offering many opportunities for nefarious actors to introduce new components to a printed circuit board (PCB). This malicious circuitry, or hardware Trojan, is designed to remain hidden and avoid post-manufacturing tests until its

functionality is triggered. The difficulty of detecting implanted hardware Trojans is compounded by an inability to compile test patterns for every feasible kind of Trojan. Current safeguards against such hidden hardware Trojans rely on individual methods for monitoring behavior changes against a known good ("golden") sample, and these methods, having been limited to single-thread environments, may not sufficiently scale to a complex COTS system. The goal of a future topic in this area would be to identify and demonstrate technical feasibility for real-time detection against hardware Trojans installed in complex COTS circuit boards. Technologies of interest could involve any of the following: single-stream or multi-modal sensing, side-channel extractions, trigger discovery via active stimulation, or performance-based machine learning architectures.

- **Ferroelectric Nitride Materials and Non-Volatile Memory:**
  Sc-doped AlN is a popular material for a number of device applications, such as RF filters, piezoelectric actuators, ultrasonic sensors, microphones, oscillators, and many more. In addition to the valuable piezoelectric and material properties of AlN-based systems, the relatively low synthesis temperatures make such materials very attractive for integration with electronics platforms compared to other piezoelectric materials, especially perovskite oxides. Recent work has demonstrated the emergence of ferroelectric switching behavior in highly Sc doped AlN thin films when the Sc percentage exceeds ~30%. This recent discovery of a ferroelectric nitride has an enormous number of potential applications in a wide variety of devices, including monolithic integration of ferroelectric non-volatile memory on CMOS; ferroelectric resistive memory; filters (e.g. Bulk Acoustic Wave and Surface Acoustic Wave); tunable RF components; switchable electro-optical components; non-volatile logic; neuromorphic memory; tunable two-dimensional electron gas (2-DEG) heterostructures; and many more. The goal of a future topic in this area could be to identify the thickness and doping ranges that exhibit ferroelectric behavior, the robustness and reproducibility of the ferroelectric response, and further demonstrate ferroelectric nitrides as a technologically useful material.

- **Massively Parallel Heterogeneous Computing:**
  For the last 50 years, advances in computing performance, cost, and ubiquity has rested on two key technology trends: 1.) Device miniaturization ("aka Moore's law") and 2.) Advances in programming methods and tools that let us leverage exponential hardware improvements while managing productivity and complexity. At the hardware level, orthogonal advances in device speeds, instruction level parallelism, and microarchitecture innovation led to aggregate performance improvements of more than 1,000,000X. At the software level, improvements in compilers, software libraries, abstraction, and collaboration led to similarly impressive productivity improvements. Unfortunately, these advances hit a brick wall around 2005 with the saturation of per processor frequency scaling and single threaded performance. Subsequent performance gains have come from hardware parallelism at the expense of programmer productivity. With transistor density and performance scaling expected to continue to taper, the expectation is that the level of parallelism, specialization, and system heterogeneity will accelerate further, making programmer productivity an even bigger challenge. Going forward, simultaneously achieving near peak performance and programming productivity in extreme heterogeneous systems will be a key challenge to enable rapid development and deployment of future hardware within the DoD SWaP constrained tactical edge. The goal of a future topic in this area could be to explore the creation of compiler technology that improves the programming productivity of massively parallel and heterogeneous processing systems.

Administrative

The Microsystems Exploration program announcement, DARPA-PA-19-04, was published on fbo.gov (click link) on July 10, 2019. Any future μE topic Pre-Solicitation Notices will be posted on fbo.gov, and posted on darpa.mil under "Work With Us" opportunities for MTO. Additional μE topic areas beyond those preliminarily addressed here are not planned to be announced by subsequent Special Notices.

All administrative questions regarding this notice must be emailed to DARPA-PA-19-04@darpa.mil. DARPA will post an FAQ on the DARPA/MTO Opportunities page at (http://www.darpa.mil/work-with-us/opportunities). The list will be updated on an ongoing basis until the close of the Microsystems Exploration program announcement.

This Special Notice is issued solely for information and potential new program planning purposes. The notice does not constitute a formal solicitation for proposals or proposal abstracts, any so sent will be disregarded. Respondents are advised that DARPA is under no obligation to acknowledge receipt of the information received or provide feedback to respondents with respect to any information submitted under this Special Notice.